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PATENT
Attorney Docket No. 211178
Client Reference No. 4/HH/F32292US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Number	6,791,393 B1
Issued:	September 14, 2004
Name of Patentee:	Underhill
Title of Invention:	Anti-Jitter Circuits

Certificate
MAR 0 3 2005
of Correction

REQUEST FOR CERTIFICATE OF CORRECTION AND REPRINTING OF PATENT FOR PATENT OFFICE MISTAKE (37 CFR 1.322(a))

Mail Stop
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attn: Decision and Certificate of Correction
Branch of the Patent Issue Division

Dear Sir:

It is requested that a Certificate of Correction be issued and the patent reprinted in its entirety to correct errors found in the above-identified patent. Please amend, page one, below the title and above Background of the Invention, to include the Field of Invention portion of the patent, which was omitted in its entirety. You will note that essentially the entire claim set requires replacement. Attached hereto is a Certificate of Correction, in duplicate, which indicates the requestedcorrections. It is believed that there is no charge for this request since the applicants were not responsible for such error, as will be apparent upon a comparison of the issued patent with the application as allowed. However, the Commissioner is hereby authorized to charge any fee that may be required to Deposit Account No. 12-1216. A duplicate copy of this communication is enclosed for that purpose.

In short, claims, 1, 5 and 12 contain errors, while claims 11 - 28 are wrong in their entirety. It is noted that the patent fails to even include two of the independent claims that were allowed. The claims as shown on the attached Certificate of Correction correspond to the claims as allowed and as renumbered by the Examiner in the issue information on the file wrapper, as may be viewed on the Office website. In view of the extreme nature of the error, we respectfully request that the Letters of Patent be reprinted.

MAR 0 4 2005

Patent No. 6,791,393
Issued: September 14, 2004
Patentee: Underhill

Respectfully submitted,

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Date: February 22, 2005

Patent No. 6,791,393
Issued: September 14, 2004
Patentee: Underhill

CERTIFICATE OF MAILING

I hereby certify that this REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR PATENT OFFICE MISTAKE (37 CFR 1.322(a)) (along with any documents referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop , Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: Feb. 23, 2005 Kathleen M. Stoltz

CertCor-PTOErr (Revised 05/21/03)

PATENT
Attorney Docket No. 211178
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Number 6,791,393 B1

Issued: September 14, 2004

Name of Patentee: Underhill

Title of Invention: Anti-Jitter Circuits

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In short, claims, 1, 5 and 12 contain errors, while claims 11 - 28 are wrong in their entirety. It is noted that the patent fails to even include two of the independent claims that were allowed. The claims as shown on the attached Certificate of Correction correspond to the claims as allowed and as renumbered by the Examiner in the issue information on the file wrapper, as may be viewed on the Office website. In view of the extreme nature of the error, we respectfully request that the Letters of Patent be reprinted.

Patent No. 6,791,393
Issued: September 14, 2004
Patentee: Underhill

Respectfully submitted,

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Patent No. 6,791,393
Issued: September 14, 2004
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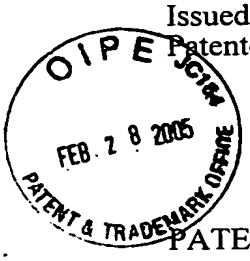

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Date: Feb. 23, 2005 Kathleen M. Stanz

CertCor-PTOErr (Revised 05/21/03)

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,791,393 B1

DATED : September 14, 2004

INVENTOR(S) : Underhill

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On page one below Title and above Background of the Invention, please insert,

FIELD OF THE INVENTION

This invention relates to anti-jitter circuits (AJC)

Replace the claims in their entirety with the following:

1. An anti-jitter circuit for reducing time jitter in an input pulse train comprising:

an integrator charge storage means for storing charge,

charging means for deriving from the input pulse train at least one charge packet during each cycle of the input pulse train and for supplying the charge packets to the integrator charge storage means,

discharging means for continuously discharging the integrator charge storage means,

the charging means and the discharging means being operative to create on the integrator charge storage means a time varying voltage,

a low pass filter coupled to said integrator charge storage means for deriving a mean d.c. voltage of said time varying voltage, and

means for comparing said time varying voltage with said mean d.c. voltage and deriving an output pulse train as a result of the comparison.

2. An anti-jitter circuit as claimed in claim 1 wherein said discharging means comprises a discharge device having a control input and said low pass filter defines a negative feedback path between the control input and an output of the integrator charge storage means whereby to maintain said mean d.c. voltage substantially constant.

3. An anti-jitter circuit as claimed in claim 2 wherein said discharge device is a current source or a current sink.

4. An anti-jitter circuit as claimed in claim 3 wherein said discharge device is a transistor.

5. An anti-jitter circuit as claimed in claim 2 wherein said mean d.c. voltage is generated at an output of said negative feedback path and said means for comparing comprises a comparator having a first input coupled to the integrator charge storage means and a second input coupled to said output of the negative feedback path.

6. An anti-jitter circuit as claimed in claim 2 further including a monostable circuit connected to the output of said means for comparing.

7. An anti-jitter circuit as claimed in claim 6 wherein said d.c. voltage is used to control the pulse length of pulses output by the monostable circuit.

8. An anti-jitter circuit as claimed in claim 7 wherein the monostable circuit is a current-controlled monostable circuit and has a control input coupled to an output of said

negative feedback path by a current mirror matched to said discharge device.

9. An anti-jitter circuit as claimed in claim 8 wherein said discharge device and said current mirror are matched transistors.

10. An anti-jitter circuit as claimed in claim 6 wherein said monostable circuit is triggered whenever a discharge part of the time-varying voltage crosses the mean d.c. voltage.

11. An anti-jitter circuit as claimed in claim 2 including means providing a low impedance path between the input and the output of the negative feedback path.

12. An anti-jitter circuit as claimed in claim 11 wherein said low impedance path is formed by diodes connected back-to-back.

13. An anti-jitter circuit as claimed in claim 1 wherein the low pass filter comprises the combination of a resistor and a capacitor.

14. An anti-jitter circuit as claimed in claim 1, wherein said charging means comprises a first charging means and a second charging means for deriving the charge packets respectively from the rising and falling edges of the input pulse train, said first and second charging means being effective as a frequency doubling means.

15. An anti-jitter circuit as claim in claim 1 further including means for

maintaining the charge value of the charge packets substantially constant.

16. An anti-jitter circuit as claimed in claim 15 wherein said means for maintaining comprises a further transistor coupled between said charging means and said integrator charge storage means.

17. An anti-jitter circuit as claimed in claim 16 wherein said further transistor is arranged to operate in grounded base mode.

18. An anti-jitter circuit as claimed in claim 17 including averaging means connected to the base of the further transistor.

19. An anti-jitter circuit as claimed in claim 16 wherein said discharging means includes a first field effect transistor operative as a discharge device and said further transistor is a second field effective transistor, and the gate of the first field effect transistor is connected to the gate of the second field effect transistor.

20. An anti-jitter circuit as claimed in claim 1 wherein said charging means is a charge pump.

21. An anti-jitter circuit for reducing time jitter in an input pulse train comprising:

an integrator charge storage means for storing charge,

charging means for deriving from the input pulse train at least one charge

packet during each cycle of the input pulse train and for supplying the charge packets to the integrator charge storage means,

discharging means for continuously discharging the integrator charge storage means, said discharging means comprising a discharge device having a control input,

the charging means and the discharging means being operative to create on the integrator charge storage means a time varying voltage, and

means for comparing said time varying voltage with a mean d.c. voltage and deriving an output pulse train as a result of the comparison, said means for comparing comprising a low pass filter coupled to said integrator charge storage means for deriving said mean d.c. voltage of said time varying voltage, said low pass filter comprising a resistor and a capacitor connected in series across said integrator charge storage means, said low pass filter defining a negative feedback path between the control input and an output of the integrator charge storage means whereby to maintain said mean d.c. voltage substantially constant, aid means for comparing further comprising inverted gate means having an input coupled to the integrator charge storage means and an output, and including means defining a further negative feedback path between said output of said inverted gate means and said discharging means whereby to establish said mean d.c. voltage as a switching level of said inverted gate means.

22. An anti-jitter circuit as claimed in claim 21 wherein said further negative feedback path is connected between said output of said inverted gate means and said control input of said discharge device.

23. An anti-jitter circuit as claimed in claim 22 wherein said further negative feedback path comprises a further low pass filter.

24. An anti-jitter circuit as claimed in claim 23 wherein said further low pass filter comprises the combination of a resistor and a capacitor.

25. An anti-jitter circuit as claimed in claim 21 wherein said further negative feedback path comprises a further low pass filter.

26. An anti-jitter circuit as claimed in claim 25 wherein said further low pass filter comprises the combination of a resistor and a capacitor.

27. An anti-jitter circuit for reducing time jitter in an input pulse train comprising:

an integrator charge storage means for storing charge,

charging means for deriving from the input pulse train at least one charge packet during each cycle of the input pulse train and for supplying the charge packets to the integrator charge storage means,

discharging means for continuously discharging the integrator charge storage means, said discharging means comprising a discharge device having a control input,

the charging means and the discharging means being operative to create on the integrator charge storage means a time varying voltage, and

means for comparing said time varying voltage with a mean d.c. voltage and deriving an output pulse train as a result of the comparison, said means for comparing

comprising a low pass filter coupled to said integrator charge storage means for deriving said mean d.c. voltage of said time varying voltage, said low pass filter comprising a resistor and a capacitor connected in series across said integrator charge storage means, said low pass filter defining a negative feedback path between the control input and an output of the integrator charge storage means whereby to maintain said mean d.c. voltage substantially constant, said means for comparing further comprising, inverted gate means having an input coupled to the integrator charge storage means and an output, and including a voltage source coupled to the discharging means whereby to establish said mean d.c. voltage as a switching level of said inverted gate means.

28. An anti-jitter circuit as claimed in claim 27 wherein said voltage source is connected between said output of said inverted gate means and said control input of said discharge device.

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